AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application.

1. (previously presented) A method of programming non-volatile memory, comprising:

boosting a voltage potential of a channel of a first plurality of non-volatile storage elements including a storage element to be inhibited from programming, each storage element of said first plurality is in communication with a first bit line receiving an inhibit voltage during said inhibiting;

inhibiting programming of a second plurality of non-volatile storage elements during at least a portion of said boosting, said second plurality including a storage element to be programmed, each storage element of said second plurality is in communication with a second bit line receiving an inhibit voltage during said inhibiting;

trapping at least a portion of said voltage potential in a portion of said channel associated with a first subset of said first plurality of non-volatile storage elements; and

enabling programming of said second plurality of non-volatile storage elements subsequent to said step of trapping by applying a program enable voltage on said second bit line.

2. (original) A method according to claim 1, wherein:

said step of boosting includes applying a first boosting voltage to said first subset of said first plurality of non-volatile storage elements and applying a second boosting voltage to a second subset of said first plurality of non-volatile storage elements.

3. (original) A method according to claim 2, further comprising:

lowering said second boosting voltage prior to enabling programming to said second plurality of non-volatile storage elements, said step of lowering is commenced subsequent to said step of trapping.

4. (original) A method according to claim 3, wherein:

said lowering said second boosting voltage includes lowering said second boosting voltage for a first portion of said second subset and then lowering said second boosting voltage for a second portion of said second subset.

5. (previously presented) A method of programming non-volatile memory, comprising:

boosting a voltage potential of a channel of a first group of non-volatile storage elements;

trapping at least a portion of said voltage potential in a portion of said channel associated with a first subset of said first group of non-volatile storage elements;

enabling programming of a second group of non-volatile storage elements subsequent to said step of trapping;

said step of boosting includes applying a first boosting voltage to said first subset of said first group of non-volatile storage elements and applying a second boosting voltage to a second subset of said first group of non-volatile storage elements; and

said first boosting voltage is lower than said second boosting voltage.

6. (original) A method according to claim 5, wherein:

said at least a portion of said voltage potential is higher than an isolated voltage potential of said portion of said channel associated with said first subset resulting from applying said first boosting voltage and lower than an isolated voltage potential of a portion of said channel associated with said second subset resulting from applying said second boosting voltage.

7. (original) A method according to claim 5, wherein:

said second boosting voltage is large enough to cause undesired programming of one or more non-volatile storage elements of said second subset of non-volatile storage elements when programming of said second subset is enabled.

8. (original) A method according to claim 2, wherein:

said second subset includes all storage elements of said first plurality that are not included in said first subset.

9. (previously presented) A method of programming non-volatile memory, comprising:

boosting a voltage potential of a channel of a first group of non-volatile storage elements;

trapping at least a portion of said voltage potential in a portion of said channel associated with a first subset of said first group of non-volatile storage elements;

enabling programming of a second group of non-volatile storage elements subsequent to said step of trapping;

said step of boosting includes applying a first boosting voltage to said first subset of said first group of non-volatile storage elements and applying a second boosting voltage to a second subset of said first group of non-volatile storage elements; and

said step of boosting further includes applying said first boosting voltage to a third subset of said second group of non-volatile storage elements and applying said second boosting voltage to a fourth subset of said second group of non-volatile storage elements.

10. (original) A method according to claim 9, wherein:

non-volatile storage elements of said first group share common word lines with corresponding non-volatile storage elements of said second group;

said first subset of said first group includes a non-volatile storage element to be inhibited; and

said third subset of said second group includes a non-volatile storage element to be programmed.

11. (original) A method according to claim 2, wherein:

said step of boosting includes coupling said voltage potential onto said channel by applying said first boosting voltage and said second boosting voltage.

12. (previously presented) A method according to claim 1, further comprising:

inhibiting programming of said first plurality of non-volatile storage elements during at least a portion of said step of boosting.

13. (cancelled)

14. (original) A method according to claim 1, wherein:

said step of trapping includes lowering a boosting voltage applied to at least one non-volatile storage element that bounds said first subset of non-volatile storage elements.

15. (previously presented) A method according to claim 14, wherein:

said at least one non-volatile storage element is part of said first subset of said first plurality of non-volatile storage elements.

16. (previously presented) A method according to claim 14, wherein:

said at least one non-volatile storage element is part of a second subset of said first plurality of non-volatile storage elements.

17. (original) A method according to claim 14, wherein:

said at least one non-volatile storage element includes a first storage element and a second storage element, said lowering includes lowering said boosting applied to said first non-volatile storage element prior to lowering said boosting voltage applied to said second non-volatile storage element.

18. (previously presented) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements;

said second plurality of non-volatile storage elements is a second string of NAND storage elements;

said first subset of said first plurality includes a storage element to be inhibited;

said second plurality includes a storage element to be programmed;

said storage element to be inhibited and said storage element to be programmed are both coupled to a first word line; and

said step of boosting includes applying at least one boosting voltage to said first plurality and said second plurality while inhibiting programming to said first plurality and said second plurality.

19. (previously presented) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements, said first plurality includes a second subset of non-volatile storage elements;

said second plurality of non-volatile storage elements is a second string of NAND storage elements, said second plurality includes a third and fourth subset of non-volatile storage elements;

said first subset of said first plurality includes a storage element to be inhibited;

said third subset of said second plurality includes a storage element to be programmed;

said storage element to be inhibited and said storage element to be programmed are both coupled to a first word line; and

said step of boosting includes applying a first boosting voltage to said first subset of said first plurality and said third subset of said second plurality and applying a second boosting voltage to said second subset of said first plurality and said fourth subset of said second plurality.

20. (previously presented) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements, said first plurality includes a second subset of non-volatile storage elements;

said second plurality of non-volatile storage elements is a second string of NAND storage elements, said second plurality includes a third and fourth subset of non-volatile storage elements;

said first subset of said first plurality includes a storage element to be inhibited;

said first subset of said first plurality includes at least one bounding storage element;

said third subset of said second plurality includes a storage element to be programmed;

said storage element to be inhibited and said storage element to be programmed are both coupled to a first word line;

one or more first additional word lines couple to other storage elements of said first subset of said first plurality and said third subset of said second plurality;

one or more second additional word lines couple to other storage elements of said second subset of said first plurality and said fourth subset of said second plurality;

said method further includes inhibiting programming of said first plurality of non-volatile storage elements and said second plurality of non-volatile storage elements prior to said step of boosting;

said step of boosting includes applying a first boosting voltage to said first subset of said first plurality and said third subset of said second plurality and applying a second boosting voltage to said second subset of said first plurality and said fourth subset of said second plurality;

said step of trapping includes lowering said first boosting voltage for said at least one bounding storage element; and

said method further includes lowering said second boosting voltage prior to enabling programming to said second plurality of non-volatile storage elements, said step of lowering said second boosting voltage is commenced subsequent to said step of trapping.

21. (previously presented) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements, said first plurality includes a second subset of non-volatile storage elements;

said second plurality of non-volatile storage elements is a second string of NAND storage elements, said second plurality includes a third and fourth subset of non-volatile storage elements;

said first subset of said first plurality includes a storage element to be inhibited;

said second subset of said first plurality includes at least one bounding storage element that bounds said first subset;

said third subset of said second plurality includes a storage element to be programmed;

said storage element to be inhibited and said storage element to be programmed are both coupled to a first word line;

one or more first additional word lines couple to other storage elements of said first subset of said first plurality and said third subset of said second plurality;

one or more second additional word lines couple to other storage elements of said second subset of said first plurality and said fourth subset of said second plurality;

said method further includes inhibiting programming of said first plurality of non-volatile storage elements and said second plurality of non-volatile storage elements prior to said step of boosting;

said step of boosting includes applying a first boosting voltage to said first subset of said first plurality and said third subset of said second plurality and applying a second boosting voltage to said second subset of said first plurality and said fourth subset of said second plurality;

said step of trapping includes lowering said second boosting voltage for said at least one bounding storage element; and

said method further includes lowering said second boosting voltage for all remaining storage elements of said second subset of said first plurality and said fourth subset of said second plurality prior to enabling programming to said second plurality, said step of lowering said second boosting voltage for all remaining storage elements is commenced subsequent to said step of trapping.

22. (previously presented) A method according to claim 1, wherein:

said first subset of said first plurality of non-volatile storage elements includes a storage element to be inhibited.

23. (previously presented) A method according to claim 22, wherein:

said first subset of said first plurality of non-volatile storage elements further includes a source side non-volatile storage element adjacent to said storage element to be inhibited.

24. (previously presented) A method according to claim 22, wherein:

said first subset of said first plurality of non-volatile storage elements further includes a drain side non-volatile storage element adjacent to said storage element to be inhibited.

25. (original) A method according to claim 22, wherein:

said first subset further includes two source side non-volatile storage elements adjacent to said storage element to be inhibited and two drain side non-volatile storage elements adjacent to said storage element to be inhibited.

26. (cancelled)

27. (cancelled)

28. (previously presented) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements; and

said second plurality of non-volatile storage elements is a second string of NAND storage elements.

29. (previously presented) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements and said second plurality of non-volatile storage elements are pluralities of flash memory devices.

30. (previously presented) A method according to claim 1, wherein:

said first plurality and said second plurality are part of an array of non-volatile storage elements;

said array is in communication with a host system; and

said array is removable from said host system.

31. (previously presented) A method according to claim 1, wherein:

said first plurality and said second plurality are part of an array of non-volatile storage elements;

said array is in communication with a host system; and

said array is embedded in said host system.

32. (original) A method according to claim 1, wherein:

said first plurality of non-volatile storage elements and said second plurality of non-volatile storage elements are pluralities of multi-state non-volatile storage elements.

33. (previously presented) A non-volatile memory system, comprising:

a first group of non-volatile storage elements, said first group including a first and second subset of non-volatile storage elements, said first subset of said first group including a non-volatile storage element to be inhibited;

a second group of non-volatile storage elements, said second group including a third and fourth subset of non-volatile storage elements, said third subset of said second group including a non-volatile storage element to be programmed; and

a plurality of word lines coupled to said first group and said second group to apply one or more boosting voltages to raise a voltage potential of a channel of said first group, said plurality of word lines includes a first word line coupled to said storage element to be inhibited and to said storage element to be programmed, said first word line applies a program voltage to said storage element to be programmed during a program operation, said plurality of word lines includes a first bounding word line on a source side of said first word line and a second bounding word line on a drain side of said first word line, said first and second bounding word lines have said one or more boosting voltages lowered thereon, prior to applying said program voltage on said first word line, in order to trap said voltage potential in a portion of said channel associated with said first subset of said first group.

34. (original) A memory system according to claim 33, wherein:

said plurality of word lines includes a first plurality of word lines coupled to said first subset of said first group and said third subset of said second group to apply a first boosting voltage; and

said plurality of word lines includes a second plurality of word lines coupled to said second subset of said first group and said fourth subset of said second group to apply a second boosting voltage.

35. (previously presented) A memory system according to claim 34, wherein:

said first bounding word line and said second bounding word line are part of said first plurality of word lines.

36. (previously presented) A memory system according to claim 34, wherein:

said first bounding word line and said second bounding word line are part of said second plurality of word lines.

37. (original) A memory system according to claim 34, wherein:

said voltage potential of said channel is a capacitively coupled voltage potential resulting from said first boosting voltage and said second boosting voltage.

38. (original) A memory system according to claim 34, wherein:

said voltage potential of said channel is higher than an isolated voltage potential of said portion of said channel associated with said first subset resulting from applying said first boosting voltage and lower than an isolated voltage potential of a portion of said channel associated with said second subset resulting from applying said second boosting voltage.

39. (original) A memory system according to claim 34, further comprising:

a plurality of bit lines including a first bit line coupled to said first group and a second bit line coupled to said second group, said first bit line applies a program inhibit voltage to said first group and said second bit line applies a program inhibit voltage to said second group while said second plurality of word lines applies said second boosting voltage.

40. (previously presented) A non-volatile memory system, comprising:

a first group of non-volatile storage elements, said first group including a first and second subset of non-volatile storage elements, said first subset of said first group including a non-volatile storage element to be inhibited;

a second group of non-volatile storage elements, said second group including a third and fourth subset of non-volatile storage elements, said third subset of said second group including a non-volatile storage element to be programmed;

a plurality of word lines coupled to said first group and said second group to apply one or more boosting voltages to raise a voltage potential of a channel of said first group, said plurality of word lines includes a first word line coupled to said storage element to be inhibited and to said storage element to be programmed, said first word line applies a program voltage to said storage element to be programmed during a program operation, said plurality of word lines includes at least one bounding word line having said one or more boosting voltages lowered thereon, prior to applying said program voltage on said first word line, in order to trap said voltage potential in a portion of said channel associated with said first subset of said first group, said plurality of word lines includes a first plurality of word lines coupled to said first subset of said first group and said third subset of said second group to apply a first boosting voltage, said plurality of word lines includes a second plurality of word lines coupled to said second subset of said first group and said fourth subset of said second group to apply a second boosting voltage; and

a plurality of bit lines including a first bit line coupled to said first group and a second bit line coupled to said second group, said second bit line has a program enable voltage applied thereon subsequent to said second plurality of word lines having said second boosting voltage lowered thereon.

41. (original) A memory system according to claim 40, wherein:

said second plurality of word lines has said second boosting voltage lowered thereon prior to said first word line applying said program voltage.

42. (original) A memory system according to claim 41, wherein:

said second plurality of word lines applies a lower second boosting voltage while said second bit line has a program enable voltage applied thereon.

43. (cancelled)

44. (original) A memory system according to claim 33, wherein:

said first group of non-volatile storage elements is a first string of NAND flash memory devices; and

said second group of non-volatile storage elements is a second string of NAND flash memory devices.

45. (previously presented) A memory system according to claim 33, wherein:

said first group of non-volatile storage elements and said second group of non-volatile storage elements are groups of multi-state flash memory devices.

46. (previously presented) A memory system according to claim 33, wherein:

said first group and said second group are part of an array of non-volatile storage elements;

said array is in communication with a host system; and

said array is removable from said host system.

47. (previously presented) A memory system according to claim 33, wherein:

said first group and said second group are part of an array of non-volatile storage elements;

said array is in communication with a host system; and

said array is embedded in said host system.

48. (cancelled)

49. (cancelled)

50. (cancelled)

51. (cancelled)

52. (previously presented) A method of programming non-volatile memory, comprising:

boosting a voltage potential of a channel of a first group of non-volatile storage elements and a channel of a second group of non-volatile storage elements by applying a first boosting voltage to a first plurality of word lines and a second boosting voltage to a second plurality of word lines, said first group includes a storage element to be programmed and said second group includes a storage element to be inhibited from programming, said first plurality of word lines is coupled to a first subset of non-volatile storage elements of said first group and a third subset of non-volatile storage elements of said second group of non-volatile storage elements, said second plurality of word lines is coupled to a second subset of non-volatile storage elements of said first group and a fourth subset of non-volatile storage elements of said second group;

trapping at least a portion of said voltage potential in a portion of said channel of said first group associated with said first subset of non-volatile storage elements;

lowering said second boosting voltage; and

programming said storage element to be programmed subsequent to said step of lowering said second boosting voltage, said programming includes draining at least a portion of said boosted voltage potential from said channel of said first group.

53. (previously presented) A method of programming non-volatile memory, comprising:

inhibiting programming of a first plurality of non-volatile storage elements and a second plurality of non-volatile storage elements by applying a program inhibit voltage to a first bit line in communication with each storage element of said first plurality and applying a program inhibit voltage to a second bit line in communication with each storage element of said second plurality, said first plurality including a non-volatile storage element to be inhibited, said second plurality including a non-volatile storage element to be programmed;

applying a first boosting voltage to a first subset of non-volatile storage elements of said first plurality and a second boosting voltage to a second subset of non-volatile storage elements of said first plurality to boost a voltage potential of a channel of said first plurality of non-volatile storage elements;

applying said first boosting voltage to a third subset of non-volatile storage elements of said second plurality and said second boosting voltage to a fourth subset of non-volatile storage elements of said second plurality to boost a voltage potential of a channel of said second plurality of non-volatile storage elements, said applying said first boosting voltage and said second boosting voltage is performed while inhibiting programming of said second plurality including said non-volatile storage element to be programmed;

trapping said voltage potential in a portion of said channel associated with said first subset of storage elements;

lowering said second boosting voltage for said second subset and said fourth subset; and

applying a program enable voltage to said second bit line subsequent to said step of lowering said second boosting voltage.

54. (previously presented) A method according to claim 53, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements;

said second plurality of non-volatile storage elements is a second string of NAND storage elements, said second plurality includes a third and fourth subset of non-volatile storage elements;

said first subset of said first plurality includes a storage element to be inhibited;

said first subset of said first plurality includes at least one bounding storage element;

said third subset of said second plurality includes a storage element to be programmed;

said storage element to be inhibited and said storage element to be programmed are both coupled to a first word line;

one or more first additional word lines couple to other storage elements of said first subset of said first plurality and said third subset of said second plurality;

one or more second additional word lines couple to other storage elements of said second subset of said first plurality and said fourth subset of said second plurality; and

said step of trapping includes lowering said first boosting voltage for said at least one bounding storage element.

55. (currently amended) A method according to claim 53, wherein:

said first plurality of non-volatile storage elements is a first string of NAND storage elements;

said second plurality of non-volatile storage elements is a second string of NAND storage elements, said second plurality includes a third and fourth subset of non-volatile storage elements;

said first subset of said first plurality includes said storage element to be inhibited;

said second subset of said first plurality includes at least one bounding storage element that bounds said first subset;

said third subset of said second plurality includes a storage element to be programmed;

said storage element to be inhibited and said storage element to be programmed are both coupled to a first word line;

one or more first additional word lines couple to other storage elements of said first subset of said first plurality and said third subset of said second plurality;

one or more second additional word lines couple to other storage elements of said second subset of said first plurality and said fourth subset of said second plurality;

said step of trapping includes lowering said second boosting voltage for said at least one bounding storage element; and

said step of lowering said second boosting voltage for said second subset comprises lowering said second boosting voltage for all remaining storage elements prior to programming said second plurality, said step of lowering said second boosting voltage for all remaining storage elements is commenced subsequent to said step of trapping.

56. (previously presented) The method of claim 9, wherein:

said first boosting voltage and said second boosting voltage are equal.

57. (previously presented) The method of claim 9, wherein:

said first boosting voltage is lower than said second boosting voltage.

58. (previously presented) The method of claim 40, wherein:

said first boosting voltage and said second boosting voltage are equal.

59. (previously presented) The method of claim 40, wherein:

said first boosting voltage and said second boosting voltage are not equal.